

# BLACK-BOX AND WHITE-BOX EARLY POWER INTENT SIMULATION AND VERIFICATION: TWO NOVEL APPROACHES



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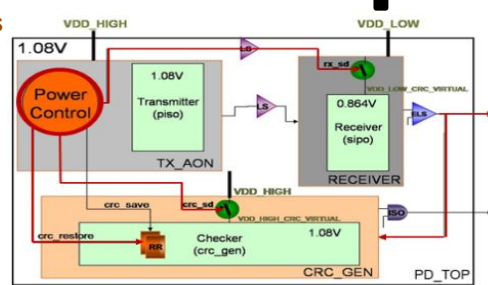


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French ANR Project HeLP

## A General Power-Aware Transaction-Level Methodology

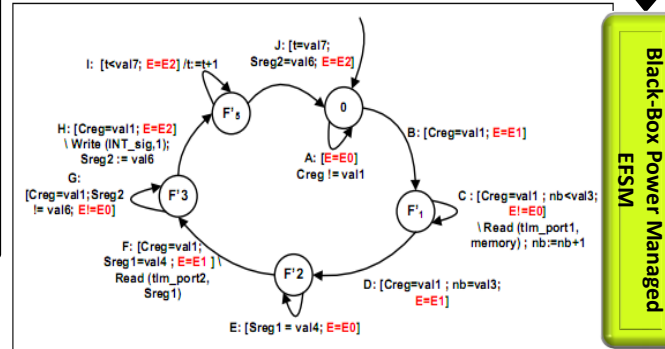
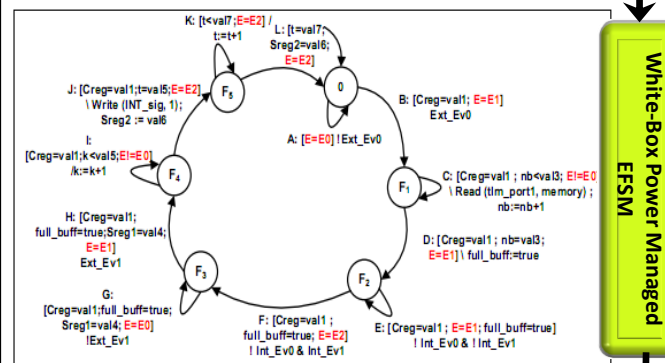
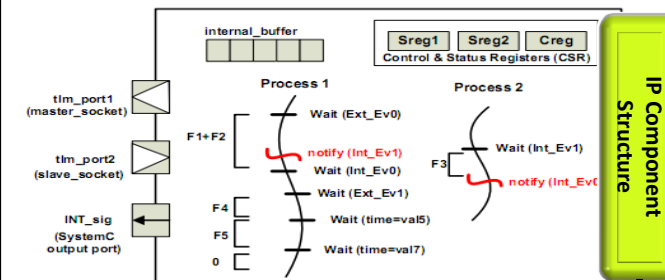
### UPF Concepts



### The Ten Requirements

Req #1	The methodology implementation should allow enabling and disabling power features dependently on the simulation aim
Req #2	Power-aware features including power intent specification as well as power estimation and control are added based on a power domain based reasoning
Req #3	The UPF (IEEE-1801) standard semantics are used as the reference to add power intent at Transaction-Level
Req #4	A Power Management Unit (PMU) should dynamically configure power domains states to set a system power mode according to a static power state table (PST) specification
Req #5	Power Control Transactions (PCTr) should be integrated with the embedded software running on the TL-platform
Req #6	All blocks involved in a power domain state change should be blocked until the PMU ends setting the requested system power mode
Req #7	Each power-gated domain needs a separate power controller which automatically controls the power down and power up sequencing
Req #8	The power management strategy as well as the PMU should be designed to use the three different power management interface
Req #9	The verification process should be power-aware and contract-based, and should dynamically check all the defined classes of contracts
Req #10	The contracts should be inserted or removed without editing the source code and a possible selective enabling of the different categories of checks (e.g. preconditions, postconditions and invariants) should be allowed.

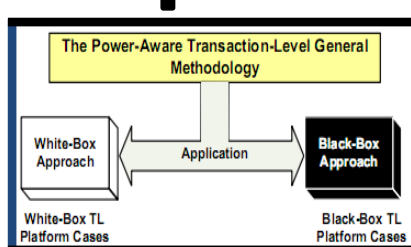
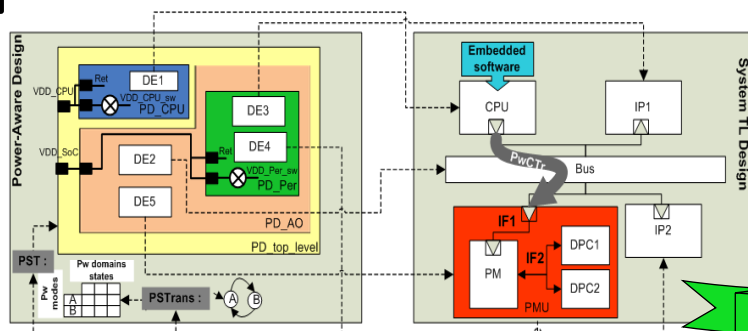
## Black-Box Vs. White-Box VPs



	White-Box	Black-Box
Sleep <sub>candidate</sub>	A, G	A, E
Ret <sub>candidate</sub>	(G, {internal_buffer, Sreg1, Creg})	(E, {Sreg1, Creg})
PwC <sub>candidate</sub>	F, J, G, A	A, E, H

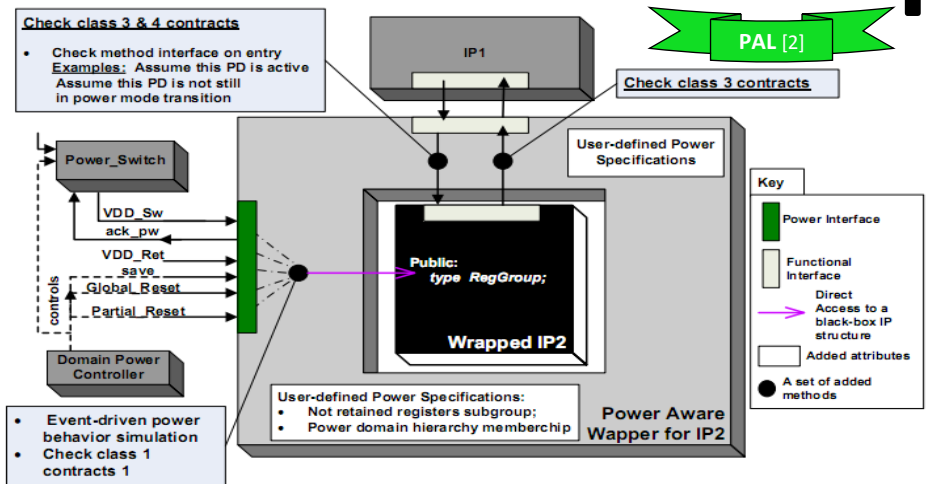
IP Component Structure  
White-Box Power Managed FSM  
Black-Box Power Managed FSM  
Power Candidates Comparison

## A White-Box Implementation Approach



PwARCH [1]

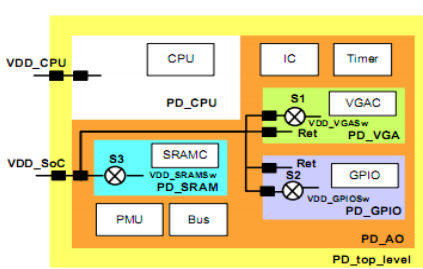
## A Black-Box Implementation Approach



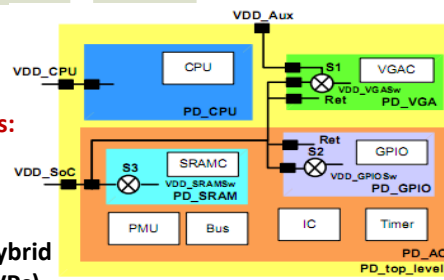
## Proof of Concept Results

Parameter	Comparison Results
Energy Savings	- 10%
SystemC Simulation Time	- 5%
PMU Activity	- 25%
Power Mode Transitions	- 35%
Running Time	+ 30%
Class 1 Checks	-28%
Class 2 Checks	- 6%
Class 3 Checks	- 8%
Class 4 Checks	-10%

+ Increase - decrease



(a) Black-Box Platform



(b) White-Box Platform

The white-box approach is:

- More accurate -> less fast
- More flexible

The black-box approach is:

- More limited
- More fast
- More generic (Ideally applied to hybrid VPs)

## References

- O. Mbarek, A. Pegatoquet, M. Auguin, "A methodology for power-aware transaction-level models of systems-on-chip using UPF standard concepts", PATMOS 2011.
- O. Mbarek, A. Pegatoquet, M. Auguin, H.E. Fathallah, "Power-aware wrappers for transaction-level virtual prototypes: a black box based approach", VLSID 2013.